REMARKS

Claims 1-4 are pending in this application, of which claim 1 has been amended. No new claims have been added.

The Examiner has maintained from the previous Office Action of August 12, 2002, the 35 USC §103(a) rejection of claims 1-4 as unpatentable over U.S. Patent 5,428,579 to Robinson et al. (hereinafter "**Robinson et al.**") in view of U.S. Patent 6,332,196 to Kawasaki et al. (hereinafter "**Kawasaki et al.**").

Applicants respectfully traverse this rejection.

As noted in Applicants' response of November 6, 2002, **Robinson et al.** discloses a flash memory card with a power control register that is used to place certain flash memories in a power down mode.

Column 2, lines 6-12 disclose:

> One type of prior flash EPROM used in a prior flash memory card has a standby mode that disables most of the flash EPROM circuitry and reduces device power consumption. The prior flash EPROM also has an active mode. The active mode requires increased power consumption. The active mode is used when the flash EPROM is being written to, read from, or erased.

The Examiner has admitted that **Robinson et al.** does not disclose the buffer memory that data is read into and that when the amount of data stored in the memory falls below a threshold the memory card is then operated in the active mode, as recited in claim 1 of the instant application.

Kawasaki et al. discloses a disk control apparatus comprising a disk controller for

controlling a circuit which controls read operation for reading data from a disk and a CPU for controlling the circuit and the disk controller. The disk controller comprises a buffer memory for storing data for being transferred between a host and the disk controller and a notification section for notifying the CPU that a first state in which an all buffer region of the buffer memory is stored with data to be transferred to the host transmits to a second state in which a predetermined space occurs in the buffer region of the buffer memory as a result of transferring data to the host. The CPU comprises a main control section for stopping power supply to the circuit during the first state and for supplying power to the circuit in response to a notification from the notification section.

Kawasaki et al. teaches only one powered state, which occurs only when a predetermined space occurs in the buffer region by transferring data to the host. The other state in which the buffer is completely full of data to be transferred to the host, consumes no power.

This is in contrast to the present invention, in which there are two power on states, where one is a high (active) mode for reading data from the memory card to the buffer at a high bit rate, and the other is a low (standby) mode in which the memory card waits for a next memory access while the buffer outputs data at a low rate.

Neither of the prior art references teaches, mentions or suggests the relationship between the current consumption and the respective data transfer rates of the card and the buffer, as recited in claim 1 of the instant application.

The Examiner now urges that:

> Kawasaki et al. teaches an active mode when the device is powered

> on and teaches the "standby mode" that operates at "a second current value lower than the first current value". Clearly when the R/W circuit of Kawasaki et al. is powered off the current value will be lower then the first current value. Furthermore operating the device in a low power mode would have been obvious and readily apparent to one having ordinary skill in the art depending upon the type of memory device used. If the memory device is such that being powered off destroyed the contents of the memory, then a low power mode would be used, or if the device had volatile control registers then the device couldn't be powered down either and would have to operate in a low power mode. Kawasaki et al. teaches operating the device in an active state when it's being accessed and otherwise placing the device in a standby mode to conserve energy when not being accessed.

Applicants respectfully disagree with the Examiner's characterization of the standby mode in **Kawasaki et al.** as a low power mode, when the Abstract and claims 1-4 of **Kawasaki et al.** clearly disclose a "main control means for stopping power supply to the circuit during the first state...."

Accordingly, claim 1 has been amended to recite that the low power state has a non-zero current consumption less than the first current value.

Thus, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-4, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an

appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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